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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,787	02/25/2002	Rajendra Pendse	CPAC 1010-2 US	6217

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,787	PENDSE ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/084787 Attorney's Docket #: CPAC 1010-2US
Filing Date: 2/25/02; priority to 2/27/01

Applicant: Pendse et al.

Examiner: Alexander Williams

Applicant's RCE field 3/18/04 has been acknowledged

Applicant's Amendment filed 3/18/04 has been acknowledged.

Claim 5 has been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, and with respect to claim 1, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claims 1 to 4 and 6 to 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over David et al. (Japan Patent # 2000-156457).

For example, in claim 1, David et al. (figures 1 to 3) specifically **figure 3** show a chip scale integrated circuit chip package comprising a die **10** mounted by flip chip interconnection to a first surface of a package substrate **14**, wherein the flip chip interconnection comprises solid state connections **(see the abtract's solution section)** of interconnect bumps **18** affixed to the die with interconnect pads **12** on the first surface of the substrate, and second level interconnections **16** formed on the first surface of the package substrate.

As to claims 12-17, Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to the grounds of rejection under section 103, see MPEP § 2113.

Claims 1 to 4 and 6 to 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Maeta et al. (U.S. Patent # 5,677,246).

For example, in claim 1, Maeta et al. (figures 1B to 18B) specifically **figure 11** show a chip scale integrated circuit chip package comprising a die **2** mounted by flip chip interconnection to a first surface of a package substrate **1**, wherein the flip chip interconnection comprises solid state connections **(see column 12, lines 45-53)** of interconnect bumps **1b** affixed to the die with interconnect pads **2a** on the first surface

of the substrate, and second level interconnections **1a** formed on the first surface of the package substrate.

As to claims 12-17, Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to the grounds of rejection under section 103, see MPEP § 2113.

Claims 1 to 4, 6 to 9 and 11 to 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Rolda, Jr. et al. (U.S. Patent Application Publication # 2002/0030261 A1) in view of David et al. (Japan Patent # 2000-156457).

For example, in claim 1, Rolda, Jr. et al. (figures 1 and 2) specifically figure 1 show a chip scale integrated circuit chip package **100** comprising a die **130** mounted by flip chip interconnection to a first surface **122** of a package substrate **120**, wherein the flip chip interconnection comprises solid state connections of interconnect bumps affixed to the die with interconnect pads on the first surface of the substrate, and second level interconnections **161** formed on the first surface of the package substrate. Rolda, Jr. et al. fail to explicitly show the flip chip interconnection comprises solid state connections of interconnection bumps affixed to the die with interconnection pads on the first surface of the substrate. However, Rolda, Jr. et al. does discloses the structures claimed of the chip, substrate and pads connected. Rolda, Jr et al. also teaches the use of thermomechanical stresses can be minimized when the solder balls connecting the second chip to the substrate (see page 4, paragragh [0042] to [0046]). It would be obvious to one of ordinary skill in the art to use solid state connection as a design choice.

David et al. is cited for showing a semiconductor device. Specifically, David et al. (figures 1 to 3) specifically **figure 3** show a chip scale integrated circuit chip package comprising a die **10** mounted by flip chip interconnection to a first surface of a package substrate **14**, wherein the flip chip interconnection comprises solid state connections **(see the abtract's solution section)** of interconnect bumps **18** affixed to the die with interconnect pads **12** on the first surface of the substrate, and second level interconnections **16** formed on the first surface of the package substrate for the purpose

of providing a interconnection of an integrated circuit chip and a board of a multi-chip module.

As to claims 12-17, Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use David et al.'s solid state connection to modify Rolda, Jr. et al.'s connection for the purpose of providing a interconnection of an integrated circuit chip and a board of a multi-chip module.

As to the grounds of rejection under section 103, see MPEP § 2113.

Claims 1 to 4, 6 to 10 and 12 to 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba et al. (U.S. Patent # 6,166,443) in view of David et al. (Japan Patent # 2000-156457).

For example, in claim 1, Inaba et al. **(figure 9)** show a chip scale integrated circuit chip package **21** comprises a die **24** mounted by flip chip interconnection to a first surface of a package substrate **22**, and second level interconnections **28** formed on the first surface of the package substrate. Inaba et al. fail to explicitly show the flip chip interconnection comprises solid state connections of interconnection bumps affixed to the die with interconnection pads on the first surface of the substrate. However, Rolda, Jr. et al. does discloses the structures claimed of the chip, substrate and pads connected. It would be obvious to one of ordinary skill in the art to use solid state connection as a design choice.

David et al. is cited for showing a semiconductor device. Specifically, David et al. (figures 1 to 3) specifically **figure 3** show a chip scale integrated circuit chip package comprising a die **10** mounted by flip chip interconnection to a first surface of a package substrate **14**, wherein the flip chip interconnection comprises solid state connections **(see the abtract's solution section)** of interconnect bumps **18** affixed to the die with interconnect pads **12** on the first surface of the substrate, and second level interconnections **16** formed on the first surface of the package substrate for the purpose

of providing a interconnection of an integrated circuit chip and a board of a multi-chip module.

As to claims 12-17, Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use David et al.'s solid state connection to modify Inaba et al.'s connection for the purpose of providing a interconnection of an integrated circuit chip and a board of a multi-chip module.

As to the grounds of rejection under section 103, see MPEP § 2113.

Response

Applicant's arguments filed 3/18/04 have been fully considered, but are moot in view of the new and modified grounds of rejections detailed above. Applicant's arguments in reference to Rolda have been considered but have not been found to be persuasive. The Examiner is interested in finding the final structure claimed by Applicant. The process to obtain the structure is considered as a process by process language and given little weight in a product claim.

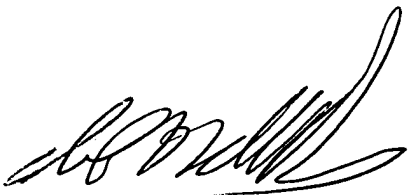
Field of Search	Date
U.S. Class and subclass: 257/686.685,723,777,778,734,737,738,784,786,787,692, 693,698	6/28/02 6/7/03 4/4/04
Other Documentation: foreign patents and literature in 257/686.685,723,777,778,734,737,738,784,786,787,692, 693,698	6/28/02 6/7/03 4/4/04
Electronic data base(s): U.S. Patents EAST	6/28/02 6/7/03 4/4/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
4/4/04



Alexander Williams
Primary Examiner